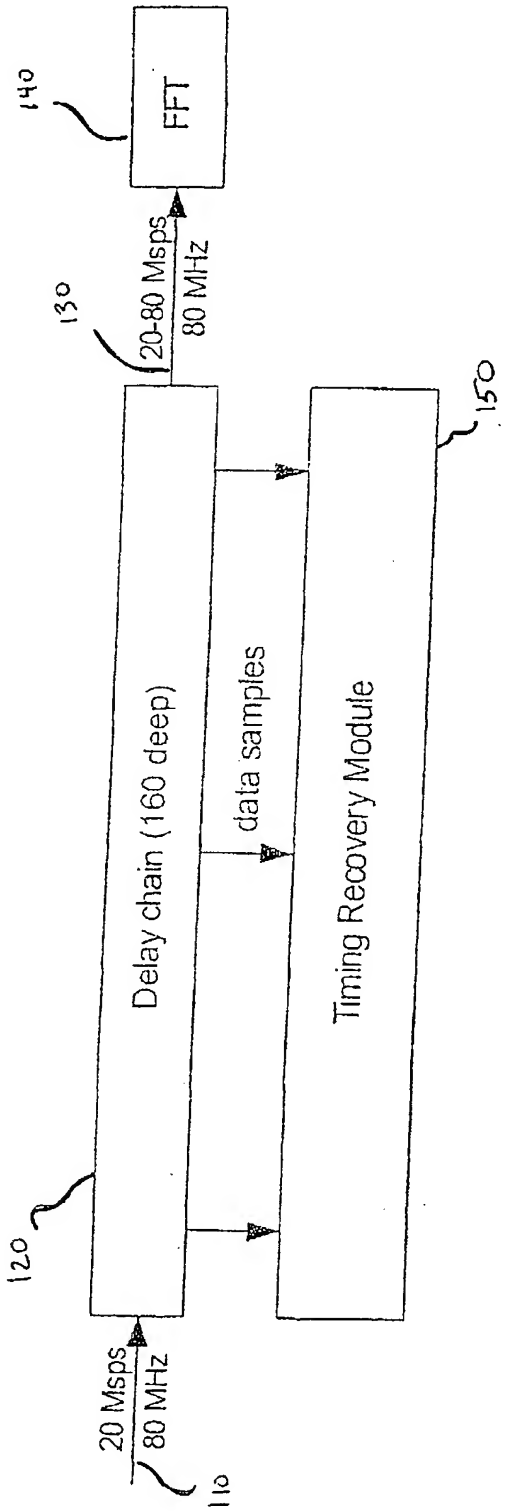
140
FFT
20-80 Msps
80 MHz
130
150
Delay chain (160 deep)
data samples
Timing Recovery Module
120
20 Msps
80 MHz
110

Figure 1

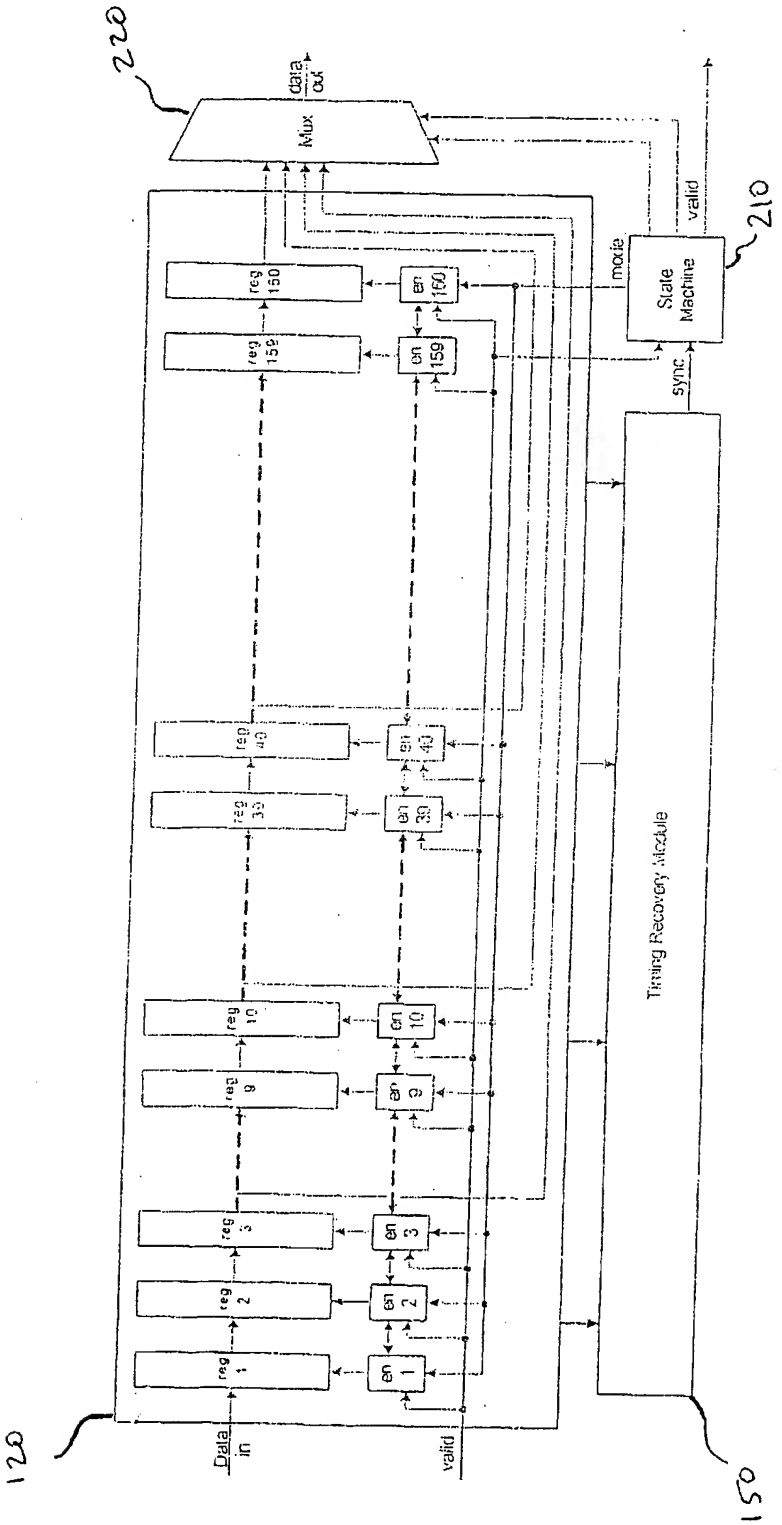
220
data out
Mux
valid
210
more
State Machine
sync
reg 160
en 160
reg 159
en 159
reg 40
en 40
reg 39
en 39
reg 10
en 10
reg 9
en 9
reg 3
en 3
reg 2
en 2
reg 1
en 1
Timing Recovery Module
120
Data in
valid
150

FIG. 2

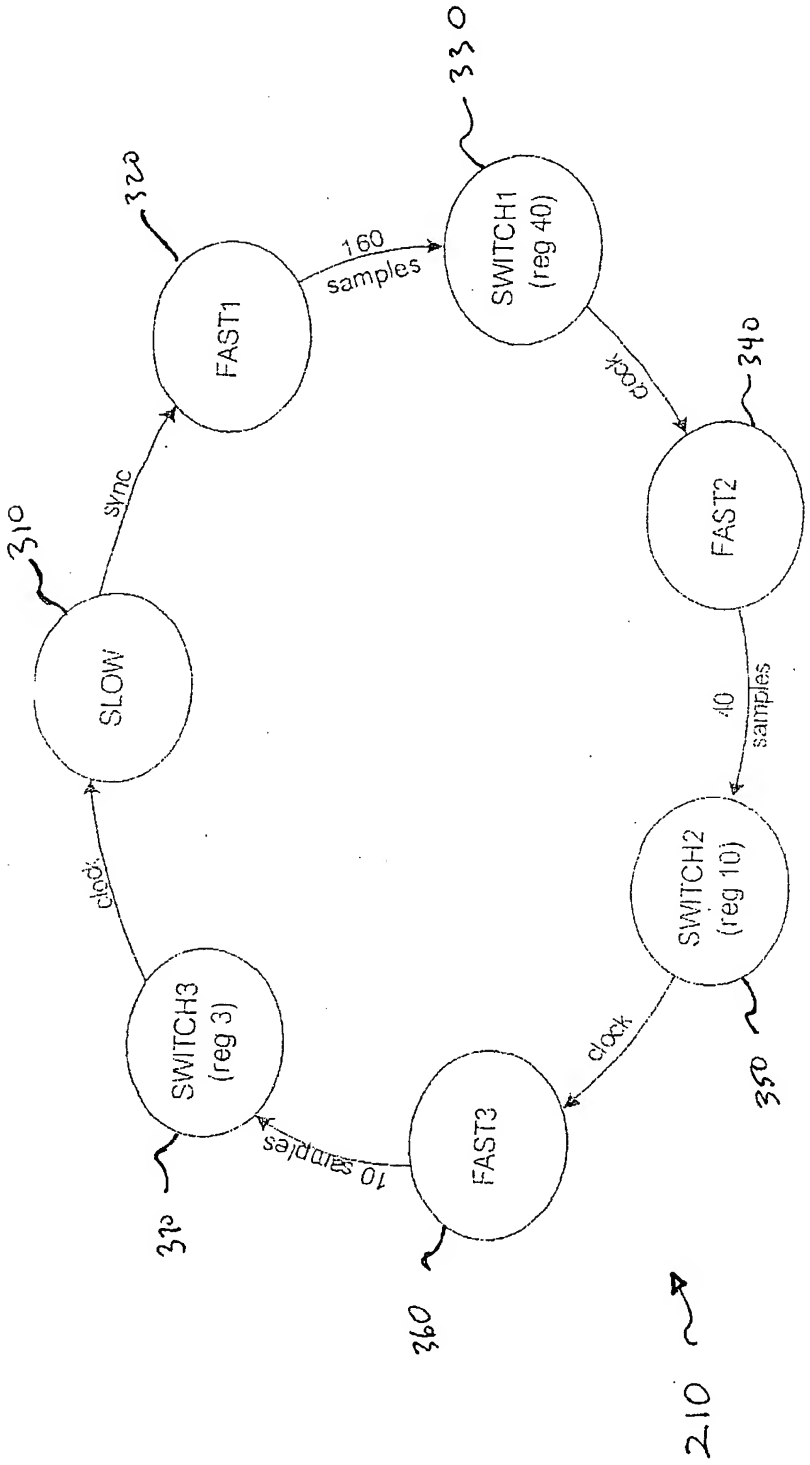
SLOW
FAST1
SWITCH1 (reg 40)
FAST2
SWITCH2 (reg 10)
FAST3
SWITCH3 (reg 3)
sync
160 samples
clock
40 samples
clock
10 samples
clock
310
320
330
340
350
360
370
210

FIG. 3

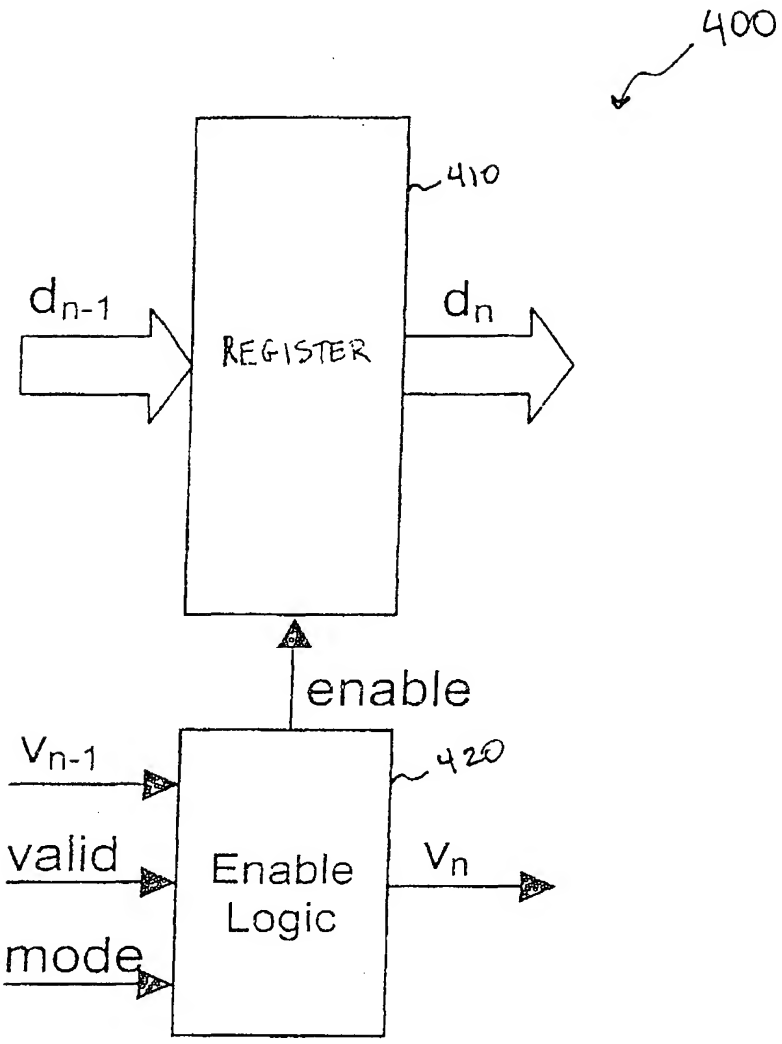
400
410
d_{n-1}
REGISTER
d_n
enable
V_{n-1}
420
valid
Enable
Logic
V_n
mode

FIG. 4

	Clock Cycle	Valid Signal (Incoming Sample at Delay Chain Input)	REGISTERS																
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
SLOW mode	1		+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	2	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
FAST mode	3		+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	4			+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	5				+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	6	+				+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
	7		+				+	+	+	+	+	+	+	+	+	+	+	+	+	+
	8		+					+	+	+	+	+	+	+	+	+	+	+	+	+
	9		+						+	+	+	+	+	+	+	+	+	+	+	+
	10	+	+							+	+	+	+	+	+	+	+	+	+	+
	11		+	+							+	+	+	+	+	+	+	+	+	+
	12		+	+								+	+	+	+	+	+	+	+	+
	13		+	+									+	+	+	+	+	+	+	+
	14	+	+	+										+	+	+	+	+	+	+
	15		+	+	+										+	+	+	+	+	+
	16		+	+	+											+	+	+	+	+
	17		+	+	+												+	+	+	+
	18	+	+	+	+													+	+	+
	19		+	+	+	+													+	+
	20		+	+	+	+														+

Fig. 5

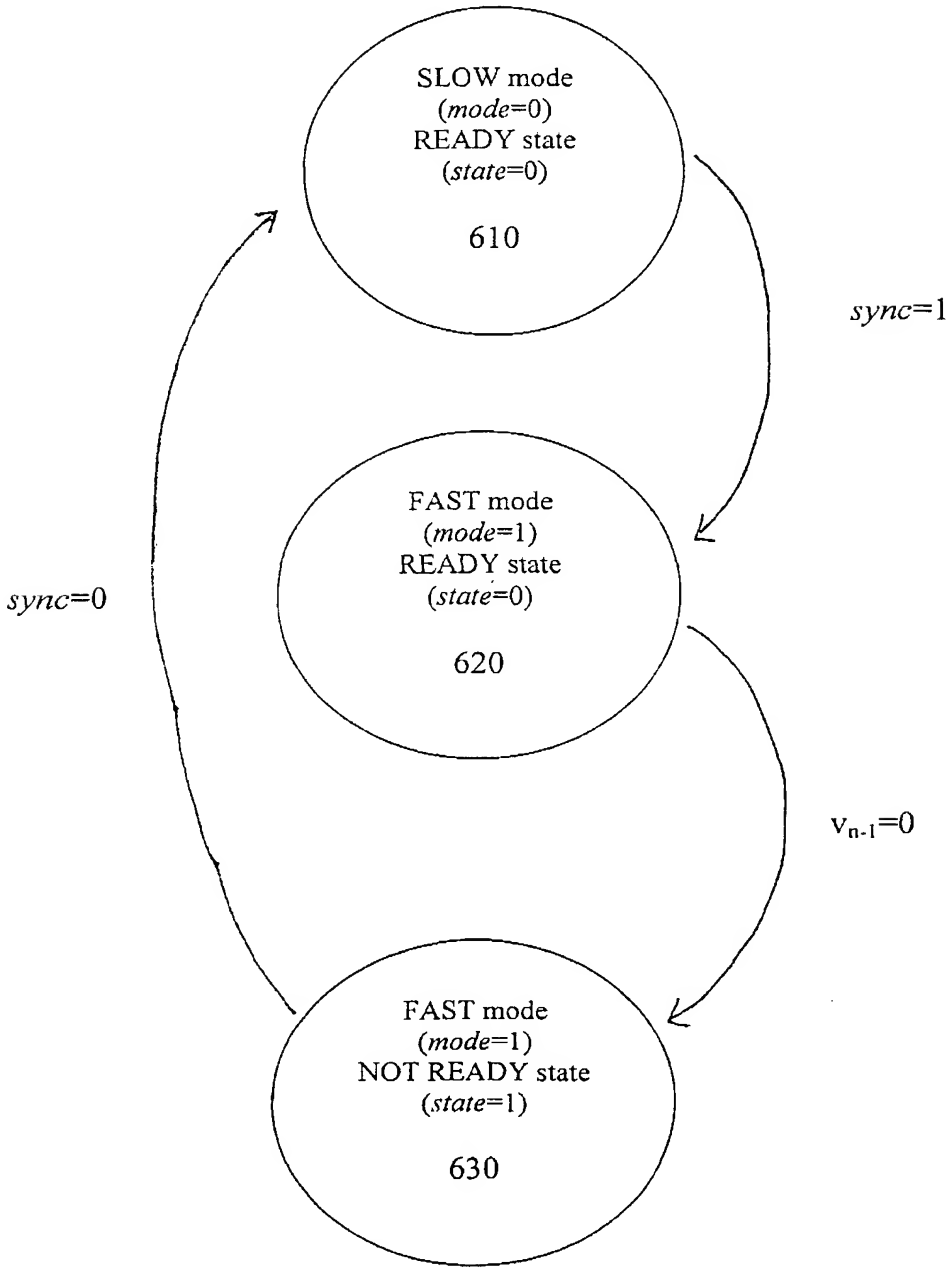
SLOW mode
(*mode*=0)
READY state
(*state*=0)
610
sync=1
FAST mode
(*mode*=1)
READY state
(*state*=0)
620
sync=0
v_{n-1}=0
FAST mode
(*mode*=1)
NOT READY state
(*state*=1)
630

FIG. 6